WHAT IS CLAIMED IS:

1. An arbiter comprising:

a bus request receiver for receiving bus request inputs from a plurality of master devices;

a priority level extractor for outputting priority level signals indicating predesignated priority levels corresponding to the plurality of master devices, if the bus requests are input through the bus request receiver, and generating a priority level summation signal indicating all priority levels of the bus requests based on the output priority level signals;

a priority output unit for outputting priority levels in order of decreasing priority based on the priority level summation signal generated by the priority level extractor;

a priority mapper comprising a master device identifier output unit for extracting identifiers of the plurality of master devices submitting bus requests based on the priority level signals and outputting the extracted master device identifiers based on the order of the priority levels output from the priority output unit; and

an arbitration circuit for granting access to a bus, to one of the plurality of master devices corresponding to the identifier output from the priority mapper.

2. The arbiter of claim 1, wherein the bus request receiver is connected to the plurality of master devices.

3. The arbiter of claim 2, wherein the bus request receiver comprises a plurality of input ports connected to the plurality of master devices for receiving bus request inputs from the plurality of master devices, and a plurality of registers provided in the plurality of input ports for storing priority levels designated for the plurality of input ports.

4. The arbiter of claim 3, wherein each of the output priority level signals is represented using the same number of bits as the priority level.

5. The arbiter of claim 4, wherein the priority level extractor performs an OR operation on one or more priority level signals on a bit-by-bit basis in order to generate the priority level summation signal, which is represented in the same number of bits as each of the one or more priority level signals.

6. The arbiter of claim 1, wherein the master device identifier output unit comprises an identifier extractor and an identifier output unit,

wherein the identifier extractor extracts a bit column requested from a matrix constructed of the priority level signals in order to generate an identifier signal, and extracts a corresponding master device identifier based on the generated identifier signal; and

wherein the identifier output unit outputs an identifier of the master device corresponding to the priority level output from the priority output unit, wherein said identifier of the master device is one of the master device identifiers extracted by the identifier extractor.

7. The arbiter of claim 6, wherein the bit column extracted by the identifier extractor includes a bit indicating a priority level.

8. The arbiter of claim 6, wherein the identifier extractor comprises one of a plurality of decoders for receiving the identifier signal in order to extract the corresponding master device identifier.

9. The arbiter of claim 7, wherein the identifier extractor comprises one of a plurality of decoders for receiving the identifier signal in order to extract the corresponding master device identifier.

10. A bus system comprising:

a bus request receiver for receiving bus request inputs from a plurality of master devices;

a priority level extractor for outputting priority level signals indicating predesignated priority levels corresponding to the plurality of master devices, if the bus requests are input through the bus request receiver, and generating a priority level summation signal indicating all priority levels of the bus requests based on the output priority level signals;

a priority output unit for outputting priority levels in order of decreasing priority based on the priority level summation signal generated by the priority level extractor;

a priority mapper comprising a master device identifier output unit for extracting identifiers of the plurality of master devices submitting bus requests in order to output the extracted master device identifiers corresponding to the priority levels output from the priority output unit; and

an arbitration circuit for granting access to a bus, to one of the plurality of master devices corresponding to the identifier output from the priority mapper.

11. The bus system of claim 10, wherein the bus request receiver is connected to the plurality of master devices.

12. The bus system of claim 11, wherein the bus request receiver comprises a plurality of input ports connected to the plurality of master devices for receiving bus request inputs from the plurality of master devices, and a plurality of registers provided in the input ports for storing priority levels designated for the input ports.

13. The bus system of claim 12, wherein each of the output priority level signals is represented using the same number of bits as the priority level.

14. The bus system of claim 13, wherein the priority level extractor performs an OR operation on one or more priority level signals on a bit-by-bit

basis in order to generate the priority level summation signal, which is represented in the same number of bits as each of the one or more priority level signals.

15. The bus system of claim 10, wherein the master device identifier output unit comprises an identifier extractor and an identifier output unit,

wherein the identifier extractor extracts a bit column requested from a matrix constructed of the priority level signals in order to generate an identifier signal, and extracts a corresponding master device identifier based on the generated identifier signal; and

wherein the identifier output unit outputs an identifier of the master device corresponding to the priority level input from the priority output unit, wherein said master device identifier is one of the master device identifiers extracted by the identifier extractor.

16. The bus system of claim 15, wherein the bit column extracted by the identifier extractor includes a bit indicating a priority level.

17. The bus system of claim 15, wherein the identifier extractor comprises one of a plurality of decoders for receiving the identifier signal, in order to extract the corresponding master device identifier.

18. The bus system of claim 16, wherein the identifier extractor comprises one of a plurality of decoders for receiving the identifier signal, in order to extract the corresponding master device identifier..